

REMARKS

In the Office Action, the Examiner rejected Claims 1, 2, 4-7, 9-12 and 14-21, which were all of the pending claims, as being fully anticipated by U.S. Patent 5,009,521 (Kosaka). The Examiner also objected to an informality in Claims 1 and 6. The previous rejection of the claims over U.S. Patent 6,181,839 (Kannon, et al.) was withdrawn.

The rejection of the claims over Kosaka is respectfully traversed for the reasons set forth below. Independent Claims 1, 6, and 11 are being amended to improve the form of these claims. Claims 1 and 6 are also being amended to correct the informality noted by the Examiner.

With respect to these informalities, the Examiner noted, in the Office Action, that Claims 1 and 6 do not identify step (e). Claim 1 is being amended to identify the detecting step as step (e), and Claim 6 is being amended to identify the repeating step of step (e). In view of these changes, the Examiner is asked to reconsider and to withdraw the objections to Claims 1 and 6.

The rejection of the claims over Kosaka is respectfully traversed because the references of record do not disclose or suggest the procedure or apparatus described in Claims 1, 6 and 11 for determining the shapes of submicron structures formed by photolithography on semiconductor wafers. Moreover, it is believed that the rejection of the claims may be based on a misinterpretation of Kosaka.

To better understand this, Applicants believe it may be helpful to review briefly this invention and the prior art.

As indicated above, the present invention, generally, relates to methods and systems for measuring submicron structures or shapes made by means of a photolithographic procedure on semiconductor wafers, and this is done by identifying pixels on a pixel array that are on the edges of those structures or shapes. Identifying those edges is a difficult challenge because these shapes can have many specific shapes, and the edges of the structures may extend in many different directions, may have curved portions, and can change directions. Because of these factors, conventional edge tracing techniques may not always be effective.

The present invention effectively addresses this difficult challenge. This is done by, first, determining an approximate edge of the shape, and identifying a set of point along that approximate edge. For each of these points, a plurality of scans in different directions are taken through substantially the point, and intensity vs. pixel information is obtained along each of these scans and in the vicinity of the edge of the shape.

Scans that have sufficient information to contain edge information are identified; and, on these identified scans, an edge detection algorithm is used to identify a point on the edge of the structure. The identified points define a more precise edge of the structure.

Kosaka discloses a procedure for processing cell images. In this procedure, the edges of the cells are detected, and these edges are used to determine other information about the cells such as cumulative chromaticity information, chromaticity histograms, cumulative gradient information and gradient histogram. Kosaka, thus, is not related to semiconductor structures.

There is, consequently, a very important difference between the present invention and the procedure disclosed in Kosaka. Kosaka relates to imaging cells, while the present invention relates to determining shapes of submicron structures formed by photolithography on semiconductor wafers.

In the Office Action, the Examiner noted that the fact that the invention related to determining shapes of submicron structures formed by photolithography on semiconductor wafers, was not given patentable weight because it was described in the preambles of Claims 1, 5 and 9. In order to give this aspect of the invention patentable weight, Claims 1, 6 and 11 are herein being amended to describe this feature positively in the body of the claims.

More specifically, Claims 1 and 11, as presented herewith, positively set forth the steps of using a photolithography process to form a submicron structure on a semiconductor wafer; and forming an electron beam image of said structure on a two-dimensional array of pixels. Claim 6, which is directed to an apparatus for extracting two-dimensional shape information from an image of a submicron structure, is being amended to describe analogous apparatus features in the body of the claim.

There are additional differences between this invention and the procedure described in Kosaka. For example, Kosaka discloses a procedure where, after a first edge pixel is found, the edge detection process uses that first edge pixel to find the next edge pixel, and then uses that next edge pixel to find the still next edge pixel. In effect this edge detection procedure traces along the edge.

This is not the procedure used in the present invention. Instead, with this invention, at each point along the approximate edge, a plurality of scans are taken, and edge information is obtained from those scans. Thus, with this invention, the detection of each edge pixel is relatively independent of the neighboring edge pixel.

This difference between the Kosaka procedure and the present invention is very important. Because of the nature of the edges that are analyzed with this invention – they change directions, move inward, move outward, and curve – a standard edge tracing algorithm – as described in Kosaka, for example – is not particularly effective. What makes this invention effective is the use of those plural scans in different directions, through the points on the approximate edge. These scans can be effectively used to detect the precise edge even if there are sudden, sharp changes in that edge. The procedure of Kosaka would not be similarly effective.

Claims 1, 6 and 11 also clearly describe the above-discussed feature of the invention. In particular, Claims 1 and 11 describe the steps of obtaining intensity vs. pixel information along a plurality of scans extending in different directions, through substantially a point along the approximate edge, recognizing scans with sufficient contrast as containing edge information, and using an edge detection algorithm to identify a point on one of those scans that is on the more precise edge location. Analogous apparatus limitations are positively set forth in Claim 6.


Thus, what is important is not that the invention uses an edge detection algorithm, but, instead, is the way the scan lines are determined that are then subjected to an edge detection algorithm. It is the use of these scan lines that enables the invention to determine effectively the edge of the image shape, even though that edge may have relatively abrupt changes.

The other references of record have been reviewed, and it is believed that these other references, whether considered individually or in combination, also fail to disclose or suggest the feature of determining these scan lines in this way for the purpose of determining the shape of a submicron structure formed on a semiconductor wafer.

Because of the above-discussed differences between independent Claims 1, 6 and 11, and because of the advantages associated with those differences, these claims patentably distinguish over the prior art and are allowable. Claims 2, 4, 5, 16 and 17 are dependent from Claim 1 and are allowable therewith; and Claims 7, 9, 10, 18 and 19 are dependent from, and are allowable with, Claim 6. Similarly, Claims 12, 14, 15, 20 and 21 are dependent from, and are allowable with, Claim 11. Accordingly, the Examiner is respectfully asked to reconsider and to withdraw the rejection of Claims 1, 2, 4-7, 9-12 and 14-21, and to allow these claims.

Every effort has been made to place this case in condition for allowance, a notice of which is requested. If the Examiner believes that a telephone conference with Applicants' Attorneys would be advantageous to the disposition of this case, the Examiner is asked to telephone the undersigned.

Respectfully Submitted,


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